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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,454	09/17/2003	Tyler J. Gomm	501283.01	8364

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EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,454	GOMM, TYLER J.	
	Examiner	Art Unit	
	Son T. Dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history*.

DETAILED ACTION

The election filed on 3/6/06 has been entered.

The election of claims 1-28 (Group I) has been acknowledged.

Claims 29-37 have been canceled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 5-8, 10, 12-14, 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kajimoto et al (U.S. Patent No 5,084,838).

Regarding claim 1, figure 1 of Kajimoto et al discloses a memory device comprising an input device (DIB), and output device (DOB), a data storage device (RAM), a processor (inherently included in Kajimoto et al since every memory device must have a microcontroller or processor so as to generate address signals, data signals and control signals to the memory device) coupled to the input device, output device, the processor includes an address bus (AB), a control bus (CB) and a data bus (DB), a memory device (UC1, UCn) coupled to the processor, the memory device including address, data and command bus (the buses connected between AB and RAM, DIB and RAM, TG and RAM), a configuration circuit (either BPC or CRB or ARB) interposed between at least one of the address (AB), control (CB) and data buses (DB).

Regarding claim 4, figure 4 of Kajimoto et al shows that the configuration circuit BPC is coupled to the address decoder CAD.

Regarding claim 5, the line between AB and ARB would be considered as a processor bus, and the line between ARB and AB would be considered as an address bus of the memory device, and the configuration circuit ARB interposed between two buses. Also, the line between DB and BPC would be considered as a data bus of the processor and the line between BPC and DIB would be considered as data bus of the memory device, and the configuration circuit BPC interposed between these two buses.

Regarding claim 6, the configuration circuit ARB is clearly coupled to the configuration control line (the line that connects to CRB).

Regarding claim 7, line between CB and CRB would be considered as a control bus of the processor, and the line between CRB and TG would be considered as the control bus of the memory device.

Regarding claim 8, the control configuration CRB is clearly coupled to the configuration control line.

Regarding claim 10, column 4, line 67 of Kajimoto et al discloses that the memory device is a DRAM.

Regarding claim 12-13, column 16, lines 41-43 teach that the memory device is a non-volatile of flash memory device.

Regarding claim 14, figure 1 of Kajimoto et al disclose a memory device comprising a memory array cell (RAM), the memory cells array coupled to to one or more signal buses (DB, CB, AB) of an external device, a configuration circuit (BPC)

interposed between the memory cell array RAM and the one or more signal buses (in this case, DB would be considered as one of them) of the external device to selectively couple portions of the one (DB) bus to the memory cell array RAM.

Regarding claim 18, figure 1 of Kajimoto et al discloses a memory device comprising an address bus (AB) coupled to the memory cell array (RAM), a data bus (DB) coupled to the memory cell array RAM, an address configuration circuit (ARB) coupled to the address bus AB, and a data configuration (BPC) coupled to the data bus DB.

Regarding claim 19, element CAD in figure 4 of Kajimoto et al is clearly an address decoder and CSW is used for reading and writing data in the memory device.

Regarding claim 20, line CB in figure 1 of Kajimoto et al is a control bus and element CRB is a control configuration circuit.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22 is rejected under 35 U.S.C. 102(e) as being anticipated by Taylor (US 2004/0024959).

For the purpose of this rejection a memory die would be considered as a memory cell array or block that has a particular capacity.

Regarding claim 22, figure 3 of Taylor discloses a memory device having a first memory die (306) having a first memory capacity, a second memory die (304) having a second memory capacity, and a configuration circuit 312) for coupling either or both of the first memory die 306 and the second memory die 304 to the external circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajimoto et al in view of McKeon (US Patent No 3,355,725).

Kajimoto et al applied as above. The only difference between Kajimoto et al and claims 2 and 15 is Kajimoto fail to disclose the use of a bi-stable relay for connecting or disconnecting a signal to a processor.

McKeon teaches that the use of a bi-stable relay (124, figure 2 or the relay in figure 3) for controlling the connection between two lines is well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kajimoto et al by using a bi-stable relay connected

between two signal lines so as to control the connection between these lines as taught by McKeon.

Regarding claim 11, the application of an address bus, data bus and control bus in an SRAM would have been obvious since it is well known in the memory art the DRAM, flash memory and SRAM could use the same address bus, data bus and control bus structure.

Claims 3, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajimoto et al in view of Lyke et al (US Patent No 6,667,873).

Kajimoto et al applied as above. The difference between kajimoto et al and claims 3, 16 and 17 is that Kajimoto et al fail to teach the use of a MEMS relay as a switch in a memory device.

Lyke (see figure 6) disclose a MEMS that performs the function of a switch in a memory device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kajimoto et al by using a MEMS relay as a switch in a memory device so as to connect or disconnect two signal lines as evidenced by Lyke et al.

Claims 23-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US 2004/0024959) in view of McKeon (US Patent No 3,355,725).

Taylor applied as above.

Regarding claim 26, the only difference between Taylor and claim 26 is that Taylor fails to teach the use of a bi-stable relay for connecting or disconnecting two signal lines. McKeon discloses a bi-stable relay that is used for connecting or

disconnecting two signal lines. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Taylor by using a bi-stable relay for connecting or disconnecting two signal lines as evidenced by McKeon.

Regarding claims 23, 24 and 28, the selection of the capacity of the first, second, third and fourth memory die would have been obvious since it just represent a design choice.

Regarding claim 25, the connection of a configuration circuit to a plurality of signal pins would have been obvious since it is well known in the art that the external signal and the internal signal in the memory device would connects through a plurality of pins.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (see above) in view of Lyke et al (US Patent No 6,667,873).

Taylor applied as above. The difference between Taylor and claim 27 is that Taylor fail to teach the use of a MEMS relay between two signal lines so as to perform the function of connecting or disconnecting these signal lines. Lyke et al disclose a MEMS relay that could be used for connecting or disconnecting two signal lines. Therefore, it would have been obvious tone of ordinary skill in the art at the time the invention was made to modify Taylor by using a MEMS relay connected between two signal lines so as to connect or disconnect these two lines as taught by Lyke et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Anderson et al disclose a memory device having a configuration circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son T. Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on Monday to Friday 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh
March 18, 2006